Van Der Waals Contact Engineering of Graphene Field-Effect Transistors for Large-Area Flexible Electronics

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ABSTRACT Graphene has great potential for high-performance flexible electronics. Although studied for more than a decade, contacting graphene efficiently, especially for large-area, flexible electronics, is still a challenge. Here, by engineering the graphene-metal van der Waals (vdW) contact, we demonstrate that ultra-low contact resistance is achievable *via* a bottom-contact

strategy incorporating a simple transfer process without any harsh thermal treatment (>150°C). The majority of the fabricated devices show contact resistances below 200 Ω·µm with values as low as 65 Ω·µm achievable. This is on a par with the state-of-the-art top- and edge-contacted graphene field-effect transistors (GFETs). Further, our study reveals that these contacts, despite the presumed weak nature of the vdW interaction, are stable under various bending conditions, thus guaranteeing compatibility with flexible electronics with improved performance. This work illustrates the potential of the previously underestimated vdW contact approach for large-area flexible electronics.

Since its discovery,[1] graphene has attracted extensive interests for various applications including sensors and RF devices.[2-4] Such applications require high-performance GFETs, where low contact resistance is a prerequisite.[5-8] After more than a decade of studies, contact resistance is still now regarded as one of the bottlenecks for realizing high-performance GFETs:[5-8] although ultra-low contact resistance (< 100 Ω·μm) has been achieved by top- and edge- contact strategies (see Figure 1a), it is mostly limited within a small area so far, with the contact pattern necessarily defined by either electron-beam lithography (EBL) or delicate ozone/ion beam treatment for a clean contact interface (see Table S1).[9-16] Such bottlenecks have to be overcome in order to achieve large scale processing, productization and further applications of high-performance GFETs.

As an alternative, bottom-contact devices with a vdW interaction have been proposed recently for use in various large-area GFET applications including biosensors and chemical sensors.[17-22] Fabrication by transfer printing graphene to a pre-patterned substrate is easy, cost-effective and circumvents cumbersome lithography process for realizing contacts, which holds natural suitability for large-area electronics. Nevertheless, compared to the extensive studies on the mechanism of the top- and edge- graphene-metal contact, the fundamental impact of the vdW interaction to the contact quality has not been thoroughly studied and clearly understood, without which a better contact performance cannot be achieved. However, such study has not been done so far because of a misconception surrounding the "weak" interactions involved in the vdW contact: the existence of a vdW separation between graphene and an electrode was believed to decrease the carrier injection efficiency dramatically and lead to an inefficient contact. In fact, this premise has only been tested by a small number of preliminary bottom-contact studies, with the state-of-the-art GFET with vdW graphene-metal interaction showing a contact resistance of approximately1000 Ω·μm.[18,21] Here, by engineering the graphene-metal vdW contact with various

contact geometries, it is possible to significantly improve the contact quality, resulting in an ultra-low contact resistance (down to 65 Ω·μm and most of values under 200 Ω·μm). This result is rather competitive with the values from the state-of-the-art top- and edge-contact devices (see Table S1).

Compared to previous work on bottom contacted GFETs, this significant contact quality improvement is ensured by employing a specially optimized lithography process for the fabrication of the metal electrodes. Importantly, this process avoids the contamination by photoresist residue which is widely observed in a standard lithography process. Furthermore, with the modified fabrication process, the bottom contact geometry is optimized by addressing several fundamental but previously unanswered questions: (1) What is the influence of the geometry on the contact properties in a bottom contact device? (2) What is the range of transfer length (L_T) in these devices as the contact geometry is varied? (3) What are the major differences in carrier transport mechanism between vdW and non-vdW contacted GFETs? By answering these questions, the functionality that underpins the performance of graphene-metal vdW contacts can be elucidated. Without an opportunity to consider these factors holistically, it is rather inevitable that high contact resistance could arise in bottom-contacted GFETs.[18,21,23]

Flexible electronics is a rapidly-growing area where graphene holds great promise. Due to the thermal budget problem, most of the strategies for achieving efficient contacts are not compatible with flexible substrates.[24,25] By contrast, the vdW contact approach achieved by transfer is naturally suitable for flexible electronics since post-annealing is not required. However, as the vdW interaction is weak and highly dependent on the graphene-metal separation, whether the mechanical deformation led by bending has any effect on the electrical characteristics of graphene-metal contact held by a weak vdW force is ambiguous. The stability and suitability of proposed

vdW contacts with flexible electronics has not been carefully examined. Here, with various bending test, our study reveals that the presumed "weak" vdW force is reliable enough to hold a stable contact under various bending conditions, which indicates its compatibility for large-area flexible electronics. We believe, our work provides a deep insight into the nature of vdW contacts in GFETs and reveals their long-underestimated potential for future large-area, cost-effective electronics, both on rigid and flexible substrates.

RESULTS AND DISCUSSION

Electrical characterization of vdW contacted GFET on rigid substrate

We first investigated a bottom-contact GFET on a rigid SiO_2/Si substrate with pre-patterned four terminal electrodes (see Materials and Methods). Figure 1b illustrates a microscope image of fabricated device. Raman spectroscopy was performed on the as-transferred graphene, revealing its single layer nature with an intensity ratio of the 2D: G bands, I(2D)/I(G), of *ca*.2.75 (see Figure S1). No D peak is observed in the Raman spectrum which indicates a high-quality transfer. Gated four terminal (4T) measurements were performed by pumping a constant source to drain current between the outer two terminals (T1 and T4), I_{ds} and sensing the voltage drop ΔV between two inner voltage terminals (T2 and T3) at different gate bias voltage. The contact resistance, R_C can be extracted according to the equation:[10]

$$R_C = \frac{1}{2} \times (R_{2T} - R_{4T}) \quad (1)$$

Here, R_{2T} is the resistance between two voltage probes measured separately by a two terminal (2T) measurement and $R_{4T}=\Delta V/I_{ds}$ is the resistance between two voltage probes extracted by a 4T measurement (See Figure S2). Previous studies on bottom-contact GFETs have employed a restricted and unoptimized range of contact geometries, leading to moderate contact performance

at best. For instance, in Ref [23], when a bottom contact electrode with an effective height of ~2 nm was employed (the electrodes were deposited in a pre-etched trench), only a minor improvement in carrier injection was observed. By contrast, in Ref [18], a much increased contact height of 100 nm was used, but the contact length was fixed at 10 μm and the effect of varying this latter parameter was not investigated.

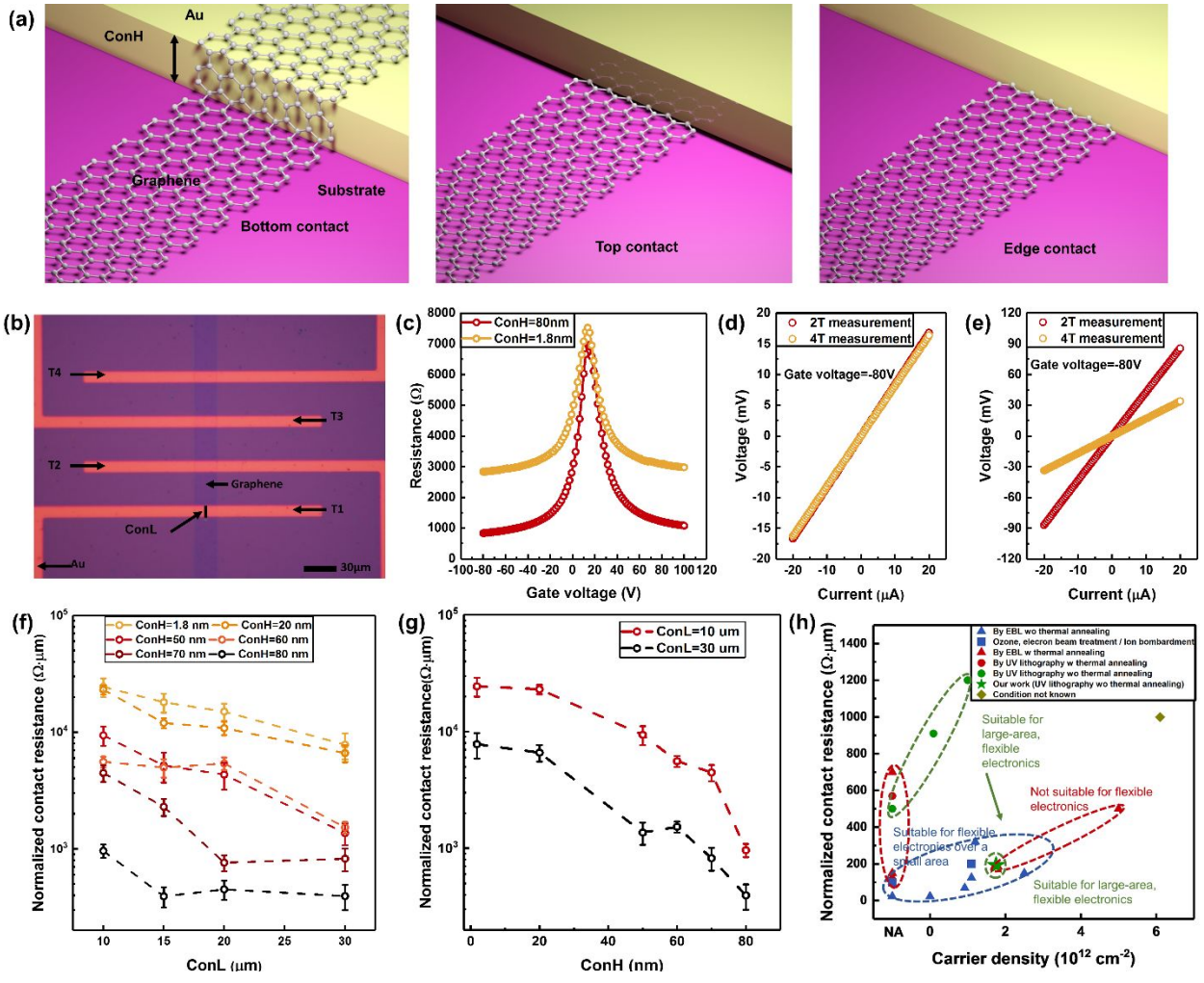

Figure 1. Electrical characterization of the GFETs with vdW contact on rigid substrate. (a) 3D schematic showing the concept of bottom, top and edge-contacts. "Substrate" refers to a silicon substrate with a 300 nm thick silicon dioxide surface layer. "Top-contact" refers to a situation where metal is evaporated or sputtered onto graphene. (b) Optical microscope image of a fabricated

graphene-based FET for gated 4T measurement. (c) Typical 2T transfer curves for measured at ConH of 80 nm and 1.8 nm (d) and (e) Output curves from 2T (red) and 4T (yellow) measurements obtained at ConH of 80 nm and 1.8 nm, respectively. (f) The statistical trend showing the change of normalized contact resistance with respect to ConH and ConL. Each data point represents the mean value of ca. 20 devices. The error bar represents the standard error. (g) The change of normalized contact resistance under different effective ConH (h) Comparison of the state-of-the-art with our work, highlighting its suitability with large-area, flexible electronics. Blue triangles, data from refs;[11,12,15,26,36] blue squares, data from refs;[14,16] red triangles, data from refs;[6,7,9,10,28,37] red circles, data from ref;[27] green circles, data from refs;[8,18,23] earthy yellow diamond, data from ref.[26]

In this work, we systematically explored the influence of the contact geometry in a bottom contact device by adjusting the contact height and length (denoted as ConH and ConL, referring to the height and the length of the contact electrodes) between 1.8 nm-80 nm and 10 μm-30 μm, respectively. Specifically, in order to obtain an effective ConH of 1.8 nm, a trench was etched in Si/SiO_2 substrate and contact metal was deposited inside. The real height of the metal in this case was 20 nm (see Ref [23] and Methods section). As shown in Figure 1c, devices with high (~80 nm) and low (~1.8 nm) effective ConH show a clear difference in the on/off ratio, which is attributed to the change of the contact quality—the on state current of devices with lower effective ConH deteriorate significantly due to a larger contact resistance.[23,26,27] This is also reflected in the output characteristics (Figure 1d and 1e). While no significant difference can be observed between 2T and 4T measurements for the device with a high effective ConH of 80 nm (Figure 1d; the ConL is 30 μm), a considerable difference is observable for the device with a low effective ConH of 1.8 nm (Figure 1e, the ConL is 30 μm). The output curve was measured at a gate voltage of -80 V with

a gate induced carrier density ~1.75×10^{12} cm^{-2}. In fact, for both a 4T measurement method and a transfer line method (TLM), the reliability of the extracted R_C depends on the homogeneity of the graphene channel.[12,28,29] Under high gate bias voltage (V_g=*-80 V* for data presented in Figure 1), the gate-induced carrier density is far larger than the fluctuation of the residual carrier density in the channel, which guarantees a reliable estimate of R_C. It should be noted that the calculated R_C also includes the contribution from the lead resistance. While this is almost negligible if the real R_C is large (under low effective ConH), it plays a significant role for those devices with a small R_C.[12] In this regard, the estimation of R_C should therefore take the lead resistance into account (see Figure S3, S4).

The extracted R_C is normalized by channel width[6,30] and plotted for different ConH and ConL (Figure 1f and 1g). Interestingly, we observe a large dependence between the normalized R_C (average) and ConL for bottom-contact devices (see Figure S5 for the distribution of the normalized contact resistance), which contradicts the result from top-contact GFETs in previous studies. In top-contacted GFETs, the normalized R_C does not change significantly with the change of ConL due to the so called "current crowding effect"[6,31]. The change in ConL in the top-contact scenario only influences the normalized R_C significantly under nanoscale contact, where ConL is much smaller than the transfer length L_T;[32] the L_T ranges from approximately 100 nm to 1.6 μm for top-contact GFETs.[28,32,33] This result indicates that for bottom-contact GFETs, especially for those devices with low ConH, the current does not crowd at the edges. The L_T is expected to be larger than 30 μm for an effective ConH of 1.8 nm (see the top curve in Figure 1f). As ConH increases, the L_T decreases (see the drop in the slope while decreasing the ConH in Figure 1f). With an effective ConH of 80 nm, no significant dependence between ConL and normalized R_C is observed, indicating the L_T is lower than 10 μm. Overall, the GFETs with a weak vdW contact

shows a much longer L_T compared to the conventional top contacted GFETs and the benefits depend on the intended applications. For example, a device with large L_T has limitations for miniaturization, but the phenomenon of local heat at contact with a large 1/f noise can be significantly reduced.[34] Since our target is high-performance, large-area electronics, the ability to decrease the contact resistance is a more important aspect to consider rather than the density/dimensions of devices. As a result, a large value of L_T in a FET is not regarded as a drawback and we thus focus on the width-normalized (Ω·μm) rather than the area-normalized (Ω·μm^2) contact resistance.

Another interesting phenomenon shown in Figure 1f and 1g is that the normalized R_C decreases with the increase of ConH as has been previously discussed in Figure 1c, 1d and 1e. With a ConH of 80 nm, 60% of devices show a contact resistance under 200 Ω·μm (ConL of 30 μm). The lowest value obtained from our devices is ~65 Ω·μm (see Figure S3, S4), which is comparable to state-of-the-art GFETs produced *via* expensive EBL process techniques,[9,28] delicate thermal annealing processes[35,36] and complex contact optimization (see Table S1).[10,37] While many contact strategies are not promising for large-area electronics, the method used in our work is well suited to this application (see Figure 1h). The only critical step is the fabrication of the metal electrodes, which employs a specially modified lithography process in order to achieve a clean metal surface without photoresist residues. (see Figure S6, S7). While this aspect has not been highlighted in previous studies,[18,21] such detail is critical for realizing a high-performance bottom contact. Given the recently developed large-area, high quality and low-cost graphene synthesis and transfer technique,[38,39] this method can be potentially extended for large-area, cost-effective GFET fabrication. We also tried to increase the ConH of the devices to 100 nm to decrease the contact resistance further. However, in this scenario, breakage of the graphene film along the contact edge

was observed, leading to a failure of the device.[40] By contrast, for the devices with ConH of 80 nm, the yield is as high as 100%. We therefore conclude that the 80 nm is an optimized value of ConH for large-area electronics.

Analysis of graphene-Au separation in vdW and non-vdW contacted devices

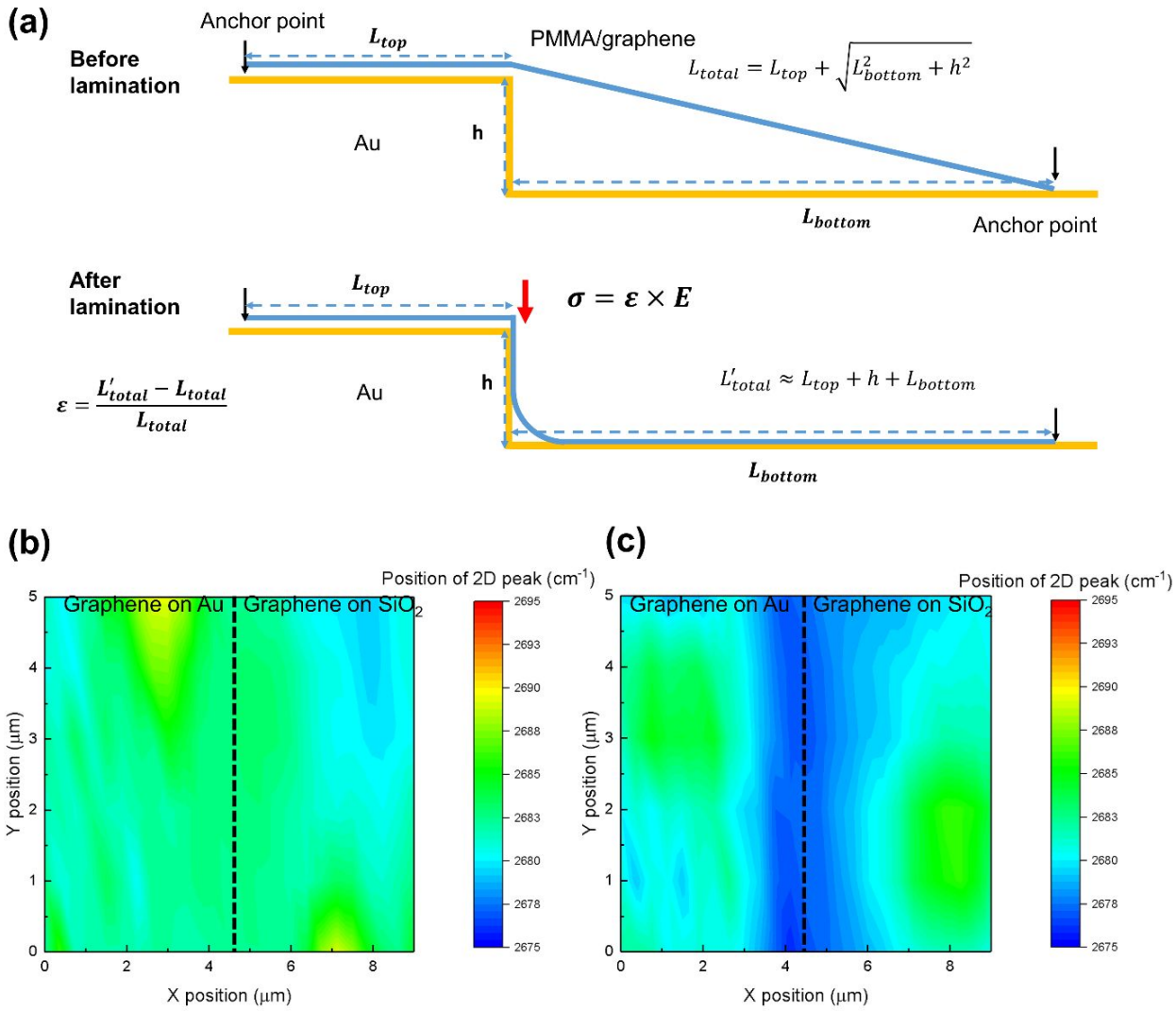

Figure 2. Raman study of the bottom contacted GFET. **(**a) Schematic illustration of the lamination process of a PMMA/graphene bilayer on to a substrate with a high step. (b) and (c) illustrate the mapping of the 2D graphene band position across the metal-dielectric interface with an effective ConH =1.8 nm and 80 nm, respectively.

To shed light on the reason for the large difference in R_C at different values of ConH, we investigated the wet transfer process of graphene for realizing the contacts. A Cu foil grown with CVD graphene was spin coated with a thin Poly (methyl methacrylate) (PMMA) layer as a mechanical support. After etching of the Cu and a proper cleaning process (see Materials and Methods), the PMMA/graphene film was transferred to a substrate pre-patterned with metal electrodes. To achieve an intimate contact between graphene and substrate, the sample was slowly heated to 150°C on a hotplate as has been previously reported.[41] This resulted in the evaporation of the transfer medium (isopropanol) and the generation of a capillary force on the film towards the substrate. Increasing the temperature above the PMMA glass transition temperature (~115°C) causes the film to change from a hard, glassy state to a rubbery state, which guaranteed a uniform, close contact between graphene and substrate and a strong, reliable vdW interaction. It is reasonable to speculate that the close contact within the vdW interaction regime was not achieved simultaneously for the entire PMMA/graphene film, but rather selected isolated areas of the film attach to the substrate in the first instance. We refer to these areas as "anchor points" and the total length between two anchor points across the metal-dielectric interface, as shown in Figure 2a, follows the equation:

$$L_{total} = L_{top} + \sqrt{L_{bottom}^2 + h^2} \qquad (2)$$

After the transfer process, the entire film forms a stable vdW interaction with the substrate separated by a vdW gap. The film was strained, and, in this scenario, the total length is given by:

$$L_{total}^{'} \approx L_{top} + h + L_{bottom} \qquad (3)$$

The localized strain in graphene across the metal-dielectric interface is further confirmed by Raman spectroscopy. Figure 2b and 2c show the results of the two-dimensional mapping of the graphene 2D band across the metal-dielectric interface, with a ConH of 1.8 nm and 80 nm,

respectively. While almost no shift of the 2D band can be observed in Figure 2b, there is a significant shift of the band in Figure 2c, which would correspond to a tensile strain of up to 0.6%.[42] Considering that the strain of the film, ε is given by:

$$\varepsilon = \frac{L'_{total} - L_{total}}{L_{total}} \qquad (4)$$

and $h = 0.08$ μm, we estimate the L_{top} and L_{bottom} to be ~ 15 μm by assuming L_{top} is equal to L_{bottom}. Under elastic deformation, the applied stress, σ is proportional to the strain according to:

$$\sigma = E \times \varepsilon \qquad (5)$$

where E denotes the Young's modulus of the PMMA film, which is *ca*. 1×10^9 Pa.[40] Therefore, the PMMA/graphene bilayer is expected to receive an applied stress of ~6×10^6 Pa (illustrated by the red arrow in Figure 2a). Such a large pressure applied to the film is expected to decrease the vdW gap between the graphene film and the Au electrode. The real case may be more complicated as it may involve a strain redistribution along the film; the analysis above only provides an approximate, semi-quantitative explanation. However, it is enough to conclude that the graphene-Au vdW contact can be engineered by transferring graphene film to metal contact with different ConH. At the same time, we monitored the intensity of the D band in the graphene Raman spectrum across the metal-dielectric interface. No significant D band was observed (see Figure S8), indicating that defects (disorder) were almost negligible in the strained graphene film. We thus believe carrier injection from defects (edge contact) is not a dominant factor in our work.

For comparison, we discuss the graphene-Au separation for the case of a top-contact GFET, which has been previously studied at the level of density functional theory.[43] In the case of a wetting metal (Co, Ni, Pd, *etc*.) evaporated on a graphene surface, the metal atoms are more aggressive while deposited and chemisorbed on the surface (by definition involving the formation of chemical bonds). The equilibrium separation between the graphene and the metal atoms is

regarded to be smaller than 2.3 Å.[23,43,44] By contrast, when a non-wetting metal (Au, Pt, Al, Cu, Ag, *etc*.) is deposited on graphene, the metal atoms are less aggressive; graphene interacts only weakly with these metal atoms, resulting mainly in physisorption (vdW interaction) at the surface. The equilibrium separation between graphene and metal atoms is thus larger (*ca*. 3.2~3.3 Å).[33,43] In previous studies, one major strategy to improve the metal-graphene contact is to minimize the equilibrium separation. This can be achieved by methods such as using Pd to form a layer of palladium-carbide at the contact interface[28,44] and exploiting the edge-contact strategy resulting from a shorter bonding distance (~1.42 Å) and a larger orbital overlap.[9] However, in terms of the bottom-contacted GFET with a vdW graphene-metal interaction, the effective separation between the *d*-orbitals of the metal and the p_z-orbitals of graphene is much larger (>3.3 Å, normally ~1 nm as suggested in Ref.[45]), which would superficially appear to result in worse contact.

Carrier transport mechanism in graphene-Au vdW and non-vdW contact

The transport mechanism in a vertical graphene-Au junction was studied to further understand the difference between vdW- and non-vdW contacted GFETs. Different transport regimes exist for carrier transport across the junction, including thermionic emission, Fowler–Nordheim tunnelling and direct tunnelling. The output characteristic from 2T and 4T measurements is linear without any rectifying behaviour. Therefore, conduction *via* thermionic emission is not considered as a dominant mechanism in graphene-metal contact.[46] Fowler–Nordheim tunnelling usually occurs under an electric field higher than 10^9 V/m.[47,48] In this work, the voltage difference between source and drain is lower than 300 mV (lower than 100 mV in a high gate doping scenario). By assuming the voltage drop on the contact equals the voltage drop on the channel, the voltage dropped on the graphene-Au junction is lower than 25 mV under a high gate bias (high channel doping) corresponding to an electric field of 2.5×10^7 V/m (assuming a vdW gap of 1 nm). This is

almost two orders of magnitudes lower than the required electric field for Fowler–Nordheim tunnelling. Thus, this phenomenon is not likely occurring in our devices. We therefore attribute the vertical carrier transport in the graphene-Au vdW contact to a direct tunnelling process,[30] which has already been extensively used to describe the vertical current for graphene based vdW heterostructures.[49-51] The vertical current $I_{vertical}$ and the contact resistivity ρ_C ($\Omega \cdot \mu m^2$) of a graphene-metal vdW contact follows the equations:

$$I_{vertical} \propto \int DOS_B(E) \times DOS_T(E - e \times V) \times [f(E - e \times V) - f(E)] \times T(E) dE \quad (6)$$

$$\rho_C = \frac{k \times V}{I_{vertical}} \quad (7)$$

where E is the energy, V is the bias between graphene and Au, k is the normalization constant (μm^2), $DOS_B(E)$ and $DOS_T(E)$ represent the density of states for the bottom layer of Au and the top layer of graphene respectively, $f(E)$ is the Fermi-Dirac distribution, m^* is the tunnelling effective mass, $\hbar$ is the reduced Planck constant, ρ_C denotes the contact resistivity, and d and U are the barrier width and barrier height respectively. $T(E)$ is the is the tunnelling probability and is given by:[49]

$$T(E) \approx e^{\frac{-2d\sqrt{m^*(U - E)}}{\hbar}} \quad (8)$$

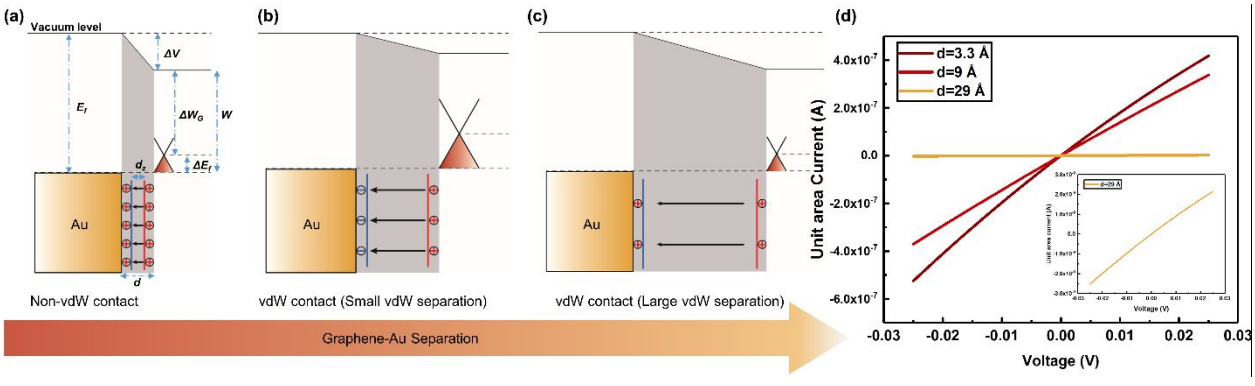

Figure 3. Graphene-metal junction under a uniform bias. Band diagram showing the Fermi level shifts due to the change of graphene-Au separation in (a) Non-vdW contact and vdW contact with (b) small and (c) large vdW separation. (d) The calculated carrier transfer characteristic in a uniformly biased graphene-Au junction.

In principle, the density of states in graphene would be zero at the Dirac point, leading to an ultra-large contact resistivity. However, when contacted with Au, graphene is doped *via* surface charge transfer, which does not modify the band structure, as a result of the dominance of weak physisorption at the surface.[43,52] Under thermal equilibrium, the relationship between the Fermi level shift ΔE_f in graphene and the graphene-metal separation d can be modelled by the method in Ref.[43] We can thus use this model to analyse the Fermi level shift under different contact scenarios (see Figure S9). In the case of a top-contact device when Au is deposited on graphene to give a graphene-Au separation of 3.3 Å (as previously discussed), the Fermi level of graphene is strongly affected by the formation of interfacial dipoles, leading to ΔE_f with a value of ~-0.103 eV (see Figure 3a and Figure S8). By contrast, in the case of a bottom-contact device with a weak vdW interaction, the graphene-Au separation is much larger (>1 nm)[45] and the interfacial dipole effects almost vanish. In this case the Au work function is determined only by the charge transfer between graphene and Au (Figure 3b). Hence, the doping of the graphene film (ΔE_f) under certain graphene-Au separation (Figure S9) is significantly larger than that seen in the top-contact case. However, further increasing the graphene-Au separation decreases the doping of graphene significantly, which means, graphene is not influenced by the existence of Au (Figure 3c). The two can be regarded as not in contact.

Considering then the contact resistivity in a simple graphene-Au junction (graphene is uniformly biased in this case), the contact resistivity is determined by the density of states of graphene as

well as the tunnel probability through the tunnel barrier. Although the equilibrium separation between graphene and Au is believed to be much larger in a vdW contact than that in a top-contact, the difference in the density of states (or ΔE_f) can compensate for the negative impact from the decrease in tunnel probability. This implies that in the case of a vdW contact with a moderate equilibrium separation, the contact resistivity can be similarly low to that in a top-contact, even though the latter has a much smaller graphene-Au separation (d and hence z_d). This can be quantitatively evaluated by fitting ΔE_f into equation (6) with different values of d. As can be seen from Figure 3d, the unit area current (representing contact resistivity) is almost the same under d = 3.3 Å and d = 9 Å. Meanwhile, further increasing d to 29 Å can lead to a decrease in both the doping level (Figure S9) and the tunnel probability, which results in a reduction in the tunnel current by two orders of magnitude.

The transport phenomenon is much more complicated in a GFET than in a uniformly biased graphene-metal contact. The carrier transported in the graphene lattice can either: (*a*) propagate horizontally within the graphene plane or (*b*) inject irreversibly into the Au electrode.[28] Here we have used a modified resistor network model to clarify this issue, assuming of total diffusive transport within the CVD graphene plane at room temperature. The schematic of the resistor network model is illustrated in Figure 4a. *V(x)* and *I(x)* refer to the voltage and current along the graphene plane and are given by:

$$\frac{dI(x)}{dx} = -\frac{V(x)}{(\frac{\rho_C}{w})} \qquad (9)$$

$$\frac{dV(x)}{dx} = -I(x)\frac{R_S}{w} \qquad (10)$$

where w is the contact width, R_S is the sheet resistance of a CVD graphene film contacted with Au and ρ_C is the contact resistivity. By combining the equations (6), (7), (8), (9), (10) and applying boundary conditions, i.e. $V(0)$=0.025 V (start of the contact), $I(L)$=0 (end of the contact), we can

calculate the change of voltage, contact resistivity and normalized contact resistance with respect to ConL (Figure 4). The ΔE_f for graphene in top-contact with Au is assumed to be -0.103 eV as previously discussed with a value of d~3.3 Å. The change in ΔE_f in bottom-contact with Au can be extracted from Figure S9 with different d. By assuming the tunnel effective mass m^* is equal to the electron mass, m_e and the tunnel barrier height is 7.8 eV,[53,54] the calculated curve fits well with most of our experimental results (Figure 4e), with d = 9 Å, 19 Å, 25.5 Å and 29 Å for bottom-contacted GFETs with effective ConH = 80 nm, 53 nm, 20 nm and 1.8 nm, respectively. The sheet resistance of graphene is assumed to be 550 Ω/□ for top-contact GFET and 150 Ω/□, 390 Ω/□, 460 Ω/□, 480 Ω/□, respectively for bottom-contact GFET with ConH values of 80 nm, 53 nm, 20 nm and 1.8 nm, respectively (since the doping level changes according to Figure S9).

Thus, the influence of ConL on the contact quality, in both top- and bottom-contact scenarios can be assessed. Assuming a local voltage bias on graphene at the start of contact (X = 0) of 0.025 V (Figure 4a), the voltage drop on graphene with varying ConL is presented in Figure 4b. The transfer length L_T in the top-contact GFET is calculated as ~1.6 μm, consistent with previous reported values of 1.4~1.65 μm for holes.[33] In contrast, L_T in a bottom-contact GFET is 3 μm when the tunnel barrier width is 9 Å (i.e. corresponding to a bottom-contact GFET with a ConH of 80 nm). As a decrease in ConH leads to an increase of the vdW gap (barrier width), the calculated L_T increases. The GFET with an effective ConH of 1.8 nm shows a L_T larger than 30 μm. In all calculated cases, the transfer length in the bottom-contact is larger than that in the top-contact. This is attributed to: (1) a smaller sheet resistance of graphene in the bottom-contact due to a higher doping level and (2) a comparable or much larger contact resistivity in the bottom-contact with various effective vdW separations. According to the classic resistor network model, a lower sheet

resistance and higher contact resistivity generate a longer transfer length. This still holds true for a graphene-metal contact and provides a means to evaluate the quality of the contact.

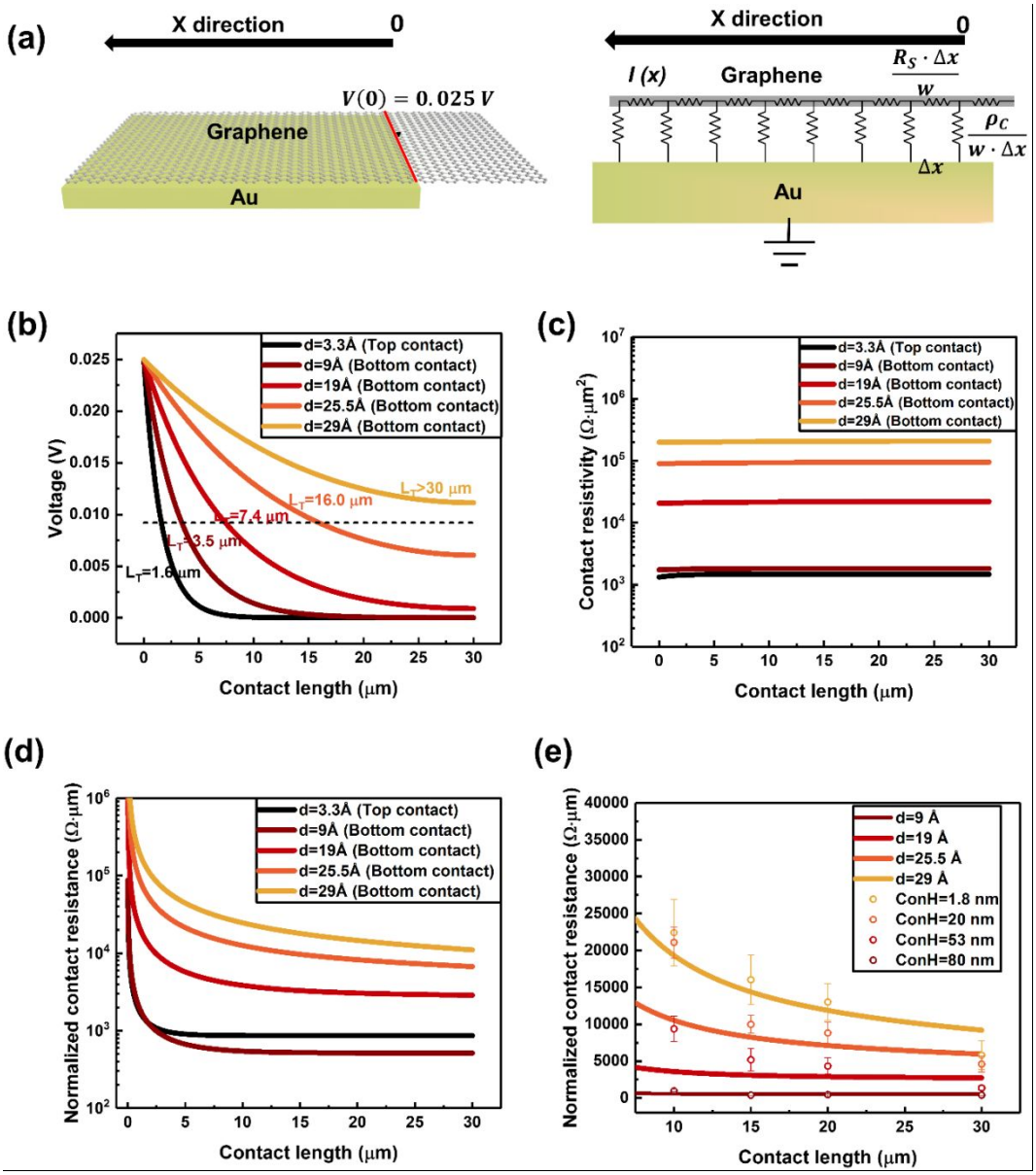

Figure 4. The electrical properties of graphene-metal contact in GFET on rigid substrate. (a) Schematic illustration of the bottom-contact geometry (left) and the corresponding resistor network model (right). (b) Calculated change of voltage for graphene in contact with Au as a function of ConL (c) Calculated change of contact resistivity for carriers injected from graphene into Au as a function of ConL. (d) and (e) Calculated change of normalized contact resistance as

a function of ConL as logarithmic and linear scales, respectively. The experimental data from Figure 1e is also plotted in (e) for a comparison between values from experiment (open circles) and calculation (solid line).

Another measure of the quality is the contact resistivity as depicted in Figure 4c, where the voltage change across a graphene-metal contact is taken into consideration. For the top-contact GFET, the calculated contact resistivity is ~950 $\Omega \cdot \mu m^2$, consistent with previously reported data.[6,55] By contrast, the contact resistivity in a bottom-contact GFET increases significantly with the widening of the vdW gap *d* from 9 Å to 29 Å. This is similar to the results in Figure 3, as the contact resistivity varies slightly over different ConL.

Finally, we discuss the normalized contact resistance, which is determined by both the transfer length and contact resistivity. Since the transfer length is positively correlated with the contact resistivity, an obvious optimum combination of a low contact resistivity with a long transfer length is not possible. In a metal-single-wall carbon nanotube contact, it has been indicated that a weak coupling (high contact resistivity) and long contact (large transfer length) is better than a strong coupling (low contact resistivity) and short contact (small transfer length).[56] Interestingly, this phenomenon is also observed in graphene-metal contacts in our work. As can be seen in Figure 4d, the normalized contact resistance in the case of a bottom-contact with ConH = 80 nm (a weak coupling but long transfer length, d = 9 Å L_T = 3 μm) shows a lower normalized contact resistance than that for a traditional top-contact (a strong coupling but short transfer length, d = 3.3 Å L_T = 1.4 μm), provided that ConL is longer than 2.5 μm. However, this rule becomes invalid when the coupling between graphene and Au is too weak, even if the L_T is larger than 30 μm in this scenario. The calculated results from this model match reasonably well with most of our experimental data, as plotted in Figure 4e. Besides, we can observe that the contact resistance from the vdW contacted

GFETs depends largely on the vdW separation between graphene and the Au contact. Based on the discussion above, two effects that co-exist and play a role on the contact resistance by decreasing the vdW gap. They are : a) the tunnelling probability of the charge carriers decreases exponentially, which decreases the contact resistivity; b) the doping of the graphene increases due to its coupling with Au.[43] Compared to the undoped graphene, doped graphene results in not only a higher tunnelling current (because of larger DOS of graphene) but also a longer transfer length. In a FET, a higher tunnelling current (lower contact resistivity) and longer transfer length can both improve the quality of the contact. This demonstrates the overall possibility of achieving low contact resistance by vdW gap engineering.

Graphene-Au vdW contact employing a flexible substrate

Many emerging applications such as wearable electronics and the internet of things require high-performance flexible electronics.[57,58] For this there is a need to develop not only new devices and components but also new fabrication techniques on flexible substrates. One of the concerns in flexible electronics is the thermal budget problem that arises as a consequence of thermally sensitive flexible substrates.[25] As no annealing is needed for bottom-contact GFETs, the devices presented herein are naturally favourable for flexible electronics. However, compared to other molecular-level interactions such as a covalent bond, vdW forces are believed to be weak and highly dependent on the vdW separation. In this regard, whether the morphological deformation (generated by bending) will lead to a change in the vdW gap and therefore lead to a significant variation in the performance of the vdW contact is not well understood yet. Such an understanding is vital if the vdW contact is going to be used in the flexible electronics and this motivated us to investigate the influence of mechanical deformation on the reliability of bottom-contacts. The device was fabricated on a polyimide (PI) film (Figure 5a). Nine measurements were performed

under different mechanical deformation states: a flat condition (A); tensile, parallel bending with bending radii of 40 mm (B) and 20 mm (D), respectively; tensile, perpendicular bending with bending radii of 40 mm (C) and 20 mm (E), respectively; compressive, parallel bending with bending radii of 40 mm (F) and 20 mm (H), respectively; compressive, perpendicular bending with bending radii of 40 mm (G) and 20 mm (I), respectively. The definition of the bending direction with respect to the channel direction is illustrated in Figure 5b. The result of typical resistance measurements for devices with high (low) effective ConH is shown in Figure 5c (f). The ConL is 30 μm for both cases and the effective ConH is ~80 nm and ~2 nm for the device tested in Figure 5c and 5f, respectively. Interestingly, the contact resistance showed no significant change under different bending regimes (Figure 5d and 5g), which likely implies a stable vdW interaction between the graphene layer and the Au electrode upon mechanical deformation. We also performed cycling tests to check the retention of contact resistance upon mechanical deformation, as shown in Figure 5e and Figure 5h for the case of high and low effective ConH, respectively. The contact resistance shows little change after 100 cycles of tensile bending (bending direction parallel to the graphene channel), with a bending radius of 40 mm. The minor variations showed in the measurements is believed to be originated from the change of contact resistance between the probe tip and the metal pad on the device. Since the device morphology varies under different bending status, the contact between the probe tip and the metal pad is likely to be changed in an uncontrollable manner. However, with existing data, it is enough to conclude that the resistance from graphene-Au vdW contact shows an insignificant change.

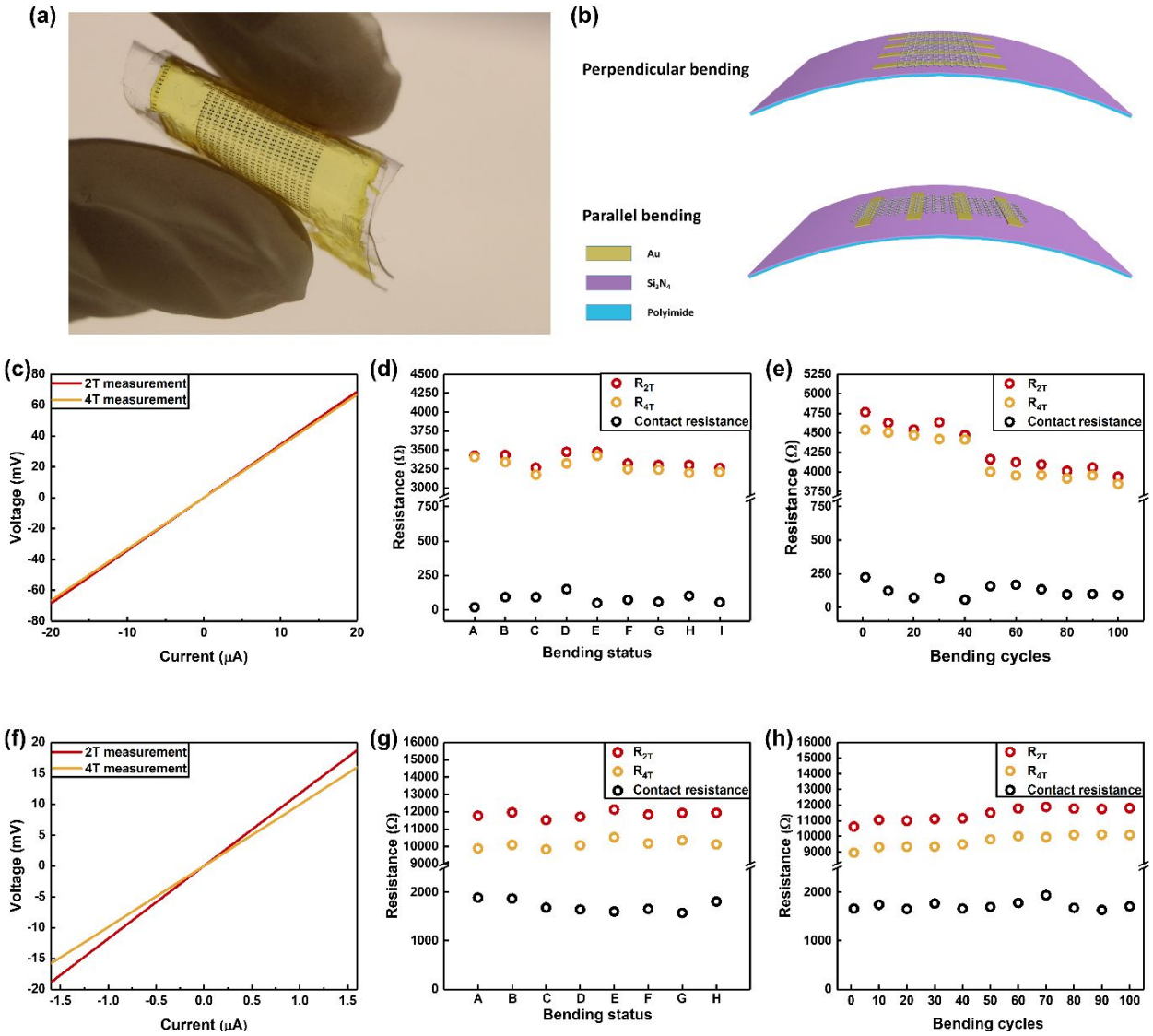

Figure 5. The electrical properties of graphene-metal contact on flexible substrate. (a) Photograph of flexible GFET under bending conditions. (b) Illustration of perpendicular and parallel bending configurations. Typical 2T and 4T measurements for devices with an effective ConH~80 nm (c) and ~2 nm (f), respectively. The ConL is 30μm in both cases. (d) The change of R_{2T} (red circles), R_{4T} (yellow circles) and contact resistance (black circles) under different bending conditions when the effective ConH is ~80 nm (d) and ~2 nm (g), respectively. The assignment of the capital letters to the different bending regimes is provided in the main text. Resistance changes under cycling

tests for a device with an effective ConH of 80 nm (e) and 2 nm (h), respectively. It should be noted that the data in (d) and (e) are taken from different devices with the same ConH and ConL.

We would like to point out that a low contact resistance is also achievable with a vdW contact approach on a flexible substrate. As shown in Figure 5d and Figure S10, the contact resistance can reach as low as 210 Ω·μm (Condition A), similar to previous values extracted on rigid substrates. It should be highlighted that this is estimated by four terminal measurement while previous work (see table S3) has employed a fitting method proposed in ref [59], which assumes a constant contact resistance for all carrier densities. It is encouraging that even when considering these inaccuracies, the previous minimum contact resistance is ~300 Ω·μm (see Table S3) and so it is indeed possible to improve on this historic value.

CONCLUSION

In conclusion, we have systematically studied the nature of graphene-metal vdW contact in GFETs, both on rigid and flexible substrates. Counterintuitively, the existence of vdW separation is found to be beneficial to the carrier injection in contacts under certain range. By engineering the vdW contact, we demonstrate that the ultralow contact resistance is achievable with a cleaner interface compared to the lithographically defined top contact. Further, the study based on vdW contacts in flexible devices shows a stable behaviour under different bending conditions, implying a promising future for vdW contact in flexible electronics. Lastly, since the performance enhancement achieved in this work is due to the non-negligible influence of metal atoms on the atomic-thick graphene, this phenomenon is also expected from the vdW contact between metal and other 2-dimensional materials. And this may benefit the development of future large-area high-performance flexible electronics.

MATERIALS AND METHODS

Fabrication of pre-patterned substrate: A p-doped silicon wafer with a 300 nm thick thermal oxide layer was used as an initial substrate. After a short treatment by hexamethyldisilazane (HMDS), photoresist S1805 (from MicroChem) was spin coated on the substrate at 4000 rpm for 30s, followed by a soft bake at 65~75 °C (not at 115°C as the standard process suggested by the supplier). After exposure and development, the sample was treated using a RIE (reactive-ion etching) process (Oxford instrument, Plasmalab 80 plus) with CHF_3 gas and Ar gas for embedding the electrode into the oxide layer if needed (for the effective ConH of 1.8 nm). The etched trench was ~20 nm deep. For the substrate with effective ConH of 20 nm, 50 nm and 80 nm, the RIE process was not needed. The NiCr alloy/Au electrode was deposited by electron-beam evaporator (Plassys, MEB400S Electron Beam Evaporator), followed by a lift-off process. The thickness of the deposited metal was ~20 nm, 20 nm, 50 nm, 80 nm for the sample with CH of 1.8 nm, 20 nm, 50 nm, 80 nm, respectively.

Transfer of graphene film onto pre-patterned substrate: Commercially available monolayer CVD-graphene on copper foil was purchased from Graphenea. A conventional PMMA-assisted transfer method was used as previously reported.[42] Before transferring the graphene onto the desired substrate, a short isopropanol (IPA) rinse was used.[60] After transfer, the sample was heated at 50 °C for 5 mins and the temperature was then gradually increased to 150 °C. The PMMA was removed by acetone and acetic acid after the transfer process.

Patterning of graphene: The as-transferred graphene film was first spin coated with a very thin layer of PMMA to serve as an interfacial layer (PMMA2041, 4%, 8000 rpm for 60 s). A layer of UV photoresist S1805 was then spin coated on top at 4000 rpm for 30 s. Exposure and development

processes were employed in order to obtain the desired pattern on top of the graphene/PMMA bilayer. Afterwards, an oxygen RIE (Oxford instrument, Plasmalab 80 plus) was used to remove excess graphene and the interfacial PMMA layer. Finally, the PMMA and photoresist was removed by acetone and rinsed by IPA to leave the patterned graphene at the surface.

Device measurement: The as-fabricated GFETs were immediately measured in ambient conditions with a Keysight B1500A semiconductor parameter analyzer. It should be noted that a post-annealing process was not adopted so that the intrinsic properties of the vdW contact could be determined.

Fabrication of flexible graphene-based resistor/GFET: A polyimide solution (PI2545 from HD Dupont) was spin coated on to a silicon/silicon dioxide substrate at 500 rpm for 5 s and twice at 2000 rpm for 60 s. Heating (by hotplate) at 140 °C for 5 minutes was employed after each spinning process. Afterwards, the PI film was cured in the oven at 250 °C for 2 hours. An isolation layer of 100 nm Si_3N_4 was deposited (using an Oxford Instruments Plasmalab System 100 ICP180) at 200 °C. Then, the fabrication of pre-patterned electrodes, graphene transfer and patterning were carried out by the same process used for FET fabrication on a rigid substrate. After fabrication, the PI film with as-fabricated devices on top was peeled off from the carrier wafer and attached to a thin Polydimethylsiloxane (PDMS) film. For the fabrication of a flexible GFET, a layer of Au bottom gate electrode of 35 nm was deposited before the Si_3N_4 deposition. Otherwise the fabrication processes were the same as described above.

Raman and atomic force microscopy (AFM) characterization of GFET: The Raman characterization was carried out with a LabRAM HR system from Horiba Jobin Yvon. A laser of 532 nm wavelength was used for the characterization of graphene samples with a power ~1 mW. For the Raman mapping experiment, the step size was 375 nm and 1 μm for the direction

perpendicular and parallel to the metal/dielectric interface, respectively. AFM characterization was carried out in ScanAsyst mode or soft-tapping mode using a Dimension Icon AFM from Bruker.

Theoretical calculation of tunnel current and contact parameters: We first calculated the tunnel current by using Equation 6. Since the Fermi level of graphene is shifted from the Dirac point (p-type doping), the I-V characteristic is asymmetric with respect to the origin point. The tunnel resistance (vertical resistance) was then determined by using Equation 7 and combined with the classic resistor network model (Equations 9 and 10). These equations were numerically integrated and evaluated until convergence was achieved in a Matlab code, under boundary conditions i.e. $V(0) = 0.025\ V$ (start of the contact), $I(L) = 0$ (end of the contact). All tunnel resistances in this work were extracted under a negative bias ($V=-0.025\ V$), where the graphene has a higher voltage bias potential than the Au electrode. However, in a real graphene device, the two cases coexist; on one side of the contact the potential of Au is higher and on the other side the potential of graphene is higher. The measured contact parameters from experiments should lie between these two extremes. We did also extract tunnel resistances under positive bias ($V=+0.025\ V$) and fed them into Equation.9 and 10. The calculated contact parameters were found to be almost the same. The calculated result is presented in Figure S13.It should be noted that our model does not account for the junction resistance for a carrier transported from graphene under metal to graphene in the channel. While this is almost negligible at high doping levels for holes because of Klein tunnelling,[61,62] it cannot be neglected for electrons. Therefore, our model is expected to offer a lower estimation of the contact resistance (or higher estimation of the vdW gap), especially when the channel region is electron-conductive. It should also be highlighted that we do not intend to extract any parameters quantitatively from this calculation since many extrinsic factors exist in the CVD graphene-based FET. Rather, the aim of this calculation is to provide a qualitative or semi-

quantitative explanation that illustrates the big difference between bottom-contact and top-contact GFETs.

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ASSOCIATED CONTENT

The authors declare no competing interests.

Supporting Information Available

Table S1. Comparison of monolayer graphene-metal contact properties at room temperature. Fig. S1. Raman spectrum of graphene transferred on Si/SiO2. Fig. S2. The device configuration for four terminal (4T) and two terminal (2T) measurements. Fig. S3. Bottom-contact GFETs with contact resistance lower than 100Ω·μm. Fig. S4. Estimation of the lead resistance. Fig. S5. Histograms of normalized contact resistance under different conditions (ConH ranges from 80 nm to 1.8 nm; ConL ranges from 30 μm to 10 μm). Fig. S6. The AFM characterization of a bottom-contact GFET at a metal-dielectric interface. Fig. S7. The characterization of bottom contact GFET with unclean metal contacts. Fig. S8. Typical Raman signal of graphene across the metal/dielectric

interface. Fig. S9. The relation between the Fermi level shift, ΔE_f and the graphene-Au separation, d calculated by the model proposed in ref. (22). Fig. S10. Typical measurement to extract contact resistance from a flexible GFET. Table S2. Comparison of device performance with the state of art CVD graphene FET. Table S3. Comparison of monolayer graphene-metal contact properties on flexible substrate at room temperature. Fig. S11. Average normalized contact resistance at a gate voltage of +100 V. Fig. S12. Typical transfer characteristics from a flexible GFET. Fig. S13. Comparison of calculated contact parameters obtained at positive and negative bias. Figure S14: The calculated contact resistance at ConL equals to L_T and $2.25L_T$, respectively.

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Author Contributions

F.L. and R.D. conceived the idea. R.D. supervised the project. F.L. performed the device fabrication and carried out the electrical characteristics measurements both on rigid and flexible substrates. N.Y. helped in the fabrication and characterization of the flexible devices. F.L. and W.T.N. performed the Raman analysis and carried out the theoretical study. W.T.N. wrote the Matlab code for numerical calculations. F.L., D.H.G. and R.D. wrote the paper, and all authors provided comments and agreed with the final form of the manuscript.

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